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10/654,893	09/05/2003	Kiyoshi Hayase	242358US2	6644

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/654,893	HAYASE, KIYOSHI	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 2-6 have been examined.

Claims 2-6 have been rejected.

Response to Arguments

1. Applicants arguments have been fully considered but are moot in view of the new grounds of rejection. The new application of the Debling reference, which Applicant has argued does not anticipate the claims (as applied previously), has been further detailed in the rejections below.

Claim Objections

2. In claim 2, the use of "respectively" in lines 3 and 5 does not convey additional limitations. Specific language stating "each executing debugging of a separate processor" or "the first unit executing debugging of a first processor and a second unit executing debugging of a second processor" would make this limitation clear.

3. In claim 2, the end of line 3 should read "executing **a** debugging" or just "executing debugging" to avoid antecedent basis problems.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2, 5 and 6 are rejected under 35 U.S.C. 112 second paragraph as being indefinite.

In claim 2, the use of "commonly" in the second-to-last line is indefinite. "Commonly" may be used to mean "frequently", in which case it should be changed to read "frequently". Or, as the examiner suspects is the case, "commonly" may be used to mean "through a common means". In this case, "provided commonly from said debugging device" only implies that the single debugging signal is not provided by multiple debugging devices (something that is probably inherent). It is generally unclear what additional limitations are intended by this amendment. The applicant is invited to contact the examiner for additional explanation regarding this rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2, 5 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Debling ('592).

6. As per claim 2, Debling ('592) discloses a multiprocessor system comprising:

a plurality of processors (Figure 2, elements 110);

a plurality of debug executing units for respectively executing the debugging of each of said plurality of processors (Figure 2, elements 120);

a plurality of controllers for respectively controlling each of said debug executing units (Figure 2, elements 140, the USB interface controller receives debug commands and each sends commands to a respective on-chip emulator 120);

a set of terminals to be connected to an external debugging device (Figure 2 element 152 is a USB connection, an external device uses this connection to control the on-chip emulators 120 to debug DSPs 110);

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged (as shown in Figure 2, a USB connection is used to send on-chip emulator commands for debugging the DSPs, because the USB allows for addressing of each individual processor (column 5 lines 42-45), the USB interfaces screen commands not intended for the USB device, collectively providing a selecting function), wherein

said plurality of processors comprise first and second processors (as shown in Figure 2),

said plurality of debug executing units comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor (as shown in Figure 2, each DSP 110 has a connected on-chip emulator 120),

said plurality of controllers comprises a first controller connected to said first debug executing unit and a second controller connected to said second debug executing unit (as shown in Figure 2, each on-chip emulator has a USB interface controller associated therewith),

said selecting circuit is connected between said first and second controllers and said set of terminals (as shown in Figure 2 and as described above, the USB interface controllers act as selecting circuitry),

said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal that is provided commonly from said debugging device through said set of terminals (as shown in Figure 2, the USB connection 152 carries commands for each on-chip emulator, the selecting function provided by the USB interface controllers 140).

7. As per claim 5, Debling ('592) discloses the multiprocessor system according to claim 2, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of setting of a given register (column 4 lines 29-31, the USB port conveys JTAG commands to each (column 5 lines 52-56) on-chip emulator. Thus the external device acting as originator of the JTAG commands

designates who receives the JTAG commands. It is inherent that the external device originating the JTAG commands uses one or more registers to process, thus one or more registers is used to determine the target for a JTAG command).

8. As per claim 6, Debling ('592) discloses the multiprocessor system according to claim 2, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of a select signal input to a given terminal from an external source (as shown in Figure 2, the USB hub 170 does not perform any selecting operations, thus it is up to the external device that sends the JTAG commands over the USB connection 152 to designate (column 5 lines 52-56) the target on-chip emulator (120)).

9. Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by Miura (US Patent 6,918,058).

Miura ('058) discloses a multiprocessor system comprising:

a plurality of processors (as shown in Figure 3, processor cores 110 and 120);

at least one debug executing unit for executing the debugging of said plurality of processors (Figure 3, debug support units 112 and 122);

at least one controller for controlling said debug executing unit (Figure 3, the debugging module 13);

a set of terminals to be connected to an external debugging device (Figure 3, the bus 30 and external debug tool 3);

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged (Figure 3, the debugging module 13 selects which processor to debug, see column 6 lines 36-39);

said plurality of processors comprise first and second processors (as shown in Figure 3);

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor (as shown in Figure 3, each processor core has a debugging support unit);

said selecting circuit is connected between said first and second debug executing units and said controller (functionally this is the case, as there is only one controller (the debugging module 13 of Figure 3 and column 6 lines 36-39), the selecting function acts on a command after the command is issued by the debugging module);

said controller is connected to said set of terminals (as shown in Figure 3, the debugging module 13 has a bus for connecting to the external debugging tool 3);

said selecting circuit inputs, to one or both of said first and second debug executing units, a debugging signal outputted from said controller (column 6 lines 36-39 and column 5 lines 50-51).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura ('058) in view of Swamy (US Patent 6,686,759).

Miura ('058) discloses a multiprocessor system comprising:

a plurality of processors (as shown in Figure 3, elements 110 and 120)

at least one debug executing unit for executing the debugging of said plurality of processors (Figure 3, element 112);

at least one controller for controlling said debug executing unit (Figure 3, element 13);

a set of terminals to be connected to an external debugging device (Figure 3, the debug bus 30); and

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged (the debug module 13 of Figure 3, see column 6 lines 34-39), wherein

said plurality of processors comprise first and second processors (as shown in Figure 3),

said debug executing unit is connected to said controller (as shown in Figure 3, debug support unit receives commands from the debugging module),

said controller is connected to said set of terminals (as shown in Figure 3, debugging module communicates with debugging tool 3 over the dedicated bus 30), and

said selecting circuit inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit (column 6 lines 36-39 and column 5 lines 50-51).

Miura ('058) does not expressly disclose the system wherein said selecting circuit is connected between said first and second processors and said debug executing unit.

Swamy ('759) teaches a system that uses demultiplexers to provide an interface between TAP signals and various processing cores (see abstract and Figure 2).

At the time of invention it would have been obvious to a person of ordinary skill in the to use the debugging support units of Miura ('058) (as shown in Figure 3) with more than one core through the use of a demultiplexor, as taught by Swamy ('759). This modification would have been obvious because having test-specific circuitry included for each processor exacerbates chip connectivity problems (Swamy ('759) column 3 lines 48-53) especially for implementations having a large number of processors (Miura ('058) column 6 lines 40-41).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

NADEEM IQBAL
PRIMARY EXAMINER